parisons and delays for 20 large PLAs from the list of 56 PLAs given in Reference 1. The average increase in area for all the PLAs given in Table 1 is 2·0%. The average increase in delay, which is analysed by the timing analyser CRYSTAL [2], is 1·04%. We must add that the increased delay is observed only on the extra outputs and the delay at the normal output of the PLA does not change.

Discussion and conclusions: A major advantage of the designs proposed in the preceding Section is that they need no modifications (extra logic) at the input of the PLA. Thus performance of a PLA is not affected by this method. Furthermore, the test set is small and independent of the personality of the PLA.

The fact that the methods proposed in this Letter can detect arbitrary bridging faults at inputs and only adjacent bit line bridging faults within the PLA, is not a major limitation generally but in folding PLAs or PLAs compacted to save silicon area this may be an important limitation. Consider a PLA with two inputs, say x_1 and x_2, such that there is no pull-down at x_{11} and x_{21}. Clearly, in such a PLA, rows x_{11} and x_{21} can be removed to save area. In the resulting PLA a bridging fault between x_{10} and x_{20} may not be detected by the tests discussed in the earlier Section. A similar situation can also arise in folding PLAs. This problem can be dealt with by another minor modification.

(i) *Design modification 3:* Introduce an extra product line *EN* which has pull-downs at the crosspoints with $x_{10}, x_{20}, \ldots, x_{n0}$. (Fig. 1*c*). This is called D3-PLA.

It can be shown that arbitrary bit lines and input bridging faults in D3-PLA can be detected by a test set $T \cup \bar{T}$, where $\bar{T}$ is obtained by complementing each bit in the test set T.

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7th April 1992

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References

1 BRAYTON, R. K., HACHTEL, G. D., MCMULLEN, C. T., and SANGIOVANNI-VINCENTELLI, A.: 'Logic minimization algorithm for VLSI synthesis' (Kluwer Academic Publishers: Boston MA, 1984)
2 OUSTERHOUT, J. K.: 'Using CRYSTAL for timing analysis'. Technical Report Document 9-12, Elect. Eng. and Comp. Science, University of California, Berkley, 1985
3 SALICK, J., UNDERWOOD, B., KUBAN, J., and MERCER, M. R.: 'An automatic test pattern generation algorithm for PLAs'. ICCAD-86, November 1986, pp. 152–155
4 SALUJA, K. K., and REDDY, S. M.: 'On detection of bridging faults in programmable logic arrays'. Int. Symp. on Electronic Devices, circuits, and systems, 1987, pp. 699–701
5 SMITH, J.: 'Detection of faults in programmable logic arrays', *IEEE Trans.*, November 1979, **C-28,** (11), pp. 845–853
6 ZHU, Z. A., and BREUER, M. A.: 'Analysis of testable PLA designs', *IEEE Design and Test of Computers*, August 1988, pp. 14–28

InGaP/GaAs/InGaP DOUBLE HETEROSTRUCTURE BIPOLAR TRANSISTORS WITH CARBON-DOPED BASE GROWN BY CBE

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Indexing terms: Bipolar devices, Transistors

Carbon-doped InGaP/GaAs/InGaP double heterostructure bipolar transistors with 25 Å setback layer are grown by chemical beam epitaxy. Transistors with nonalloyed base contacts show a very high common emitter current gain of 120 and very low collector saturation voltage of 75 mV at room temperature.

Introduction: Conventional GaAs-based heterostructure bipolar transistors (HBTs) with a wide energy gap AlGaAs emitter have demonstrated excellent device and circuit performance [1]. A large valence band offset ΔE_V at the emitter/base junction of an Npn HBT is very advantageous to effectively confine holes in the heavily-doped base. This hole confinement permits a high base-to-emitter doping ratio to enhance the high frequency performance of the HBT without sacrificing current gain [2]. Recently, there has been much interest in replacing the commonly used AlGaAs alloy with $In_{0.49}Ga_{0.51}P$, which is lattice-matched to GaAs substrate, as the wide-gap emitter for HBTs [3–7]. The aluminium-free $In_{0.49}Ga_{0.51}P$ is lattice-matched to GaAs substrate and has a bandgap energy of 1·9 eV. However, the band offset of the InGaP/GaAs heterointerface is somewhat controversial with the conduction band offset ΔE_c ranging from 30 to 390 meV [5, 8–10]. A recent report using the internal photoemission [11] of GaAs/InGaP photodiodes indicates a conduction band discontinuity of 108 meV. Nevertheless, the large valence band offset energy ($\Delta E_v \simeq 0{\cdot}3$ eV) of the $In_{0.49}Ga_{0.51}P$/GaAs heterointerface is highly desirable for HBT applications. Similar valence band discontinuity can only be obtained with a $Al_{0.6}Ga_{0.4}As$/GaAs heterointerface with high aluminium concentration and a large conduction band discontinuity. A large ΔE_c is not desirable in designing double heterojunction bipolar transistors (DHBTs) which use a wide-gap collector to enhance the breakdown voltage of the transistors. Because of the quantum reflection of the injected electrons from the potential spike at the base–collector junction, the current gain of DHBTs will be reduced, as shown in Fig. 1. Usually, a compositionally graded collector region or an extended small bandgap collector region is needed to lower the potential spike for the injected minority carriers at the base–collector interface. Minority carriers trapped by the potential barrier at the base/collector interface reduce current gain and generate an undesirable charge storage effect in the collector depletion region during large switching transients. With the smaller ΔE_c of InGaP/GaAs, very little charge accumulation is generated and the collector depletion region in the small bandgap material is reduced. The use of carbon doping promises high doping concentration in the GaAs base and a *p*-type doping concentration as high as $10^{21}\,cm^{-3}$ has been reported [12]. Compared to the commonly used Be dopants in GaAs [13], the low diffusion of carbon dopants preserves the integrity of the emitter/base heterojunction during the growth and improves the reliability of transistors [14]. In this Letter, the advantages of the large $\Delta E_V/\Delta E_C$ ratio of the InGaP/GaAs heterointerface and the high carbon-doped GaAs base are illustrated by an InGaP/GaAs/InGaP double heterojunction bipolar transistor.

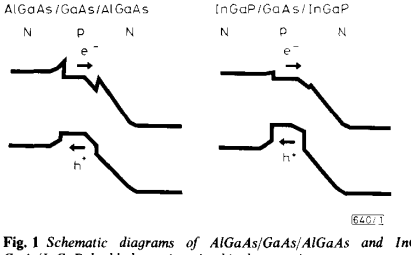

Fig. 1 *Schematic diagrams of AlGaAs/GaAs/AlGaAs and InGaP/GaAs/InGaP double heterojunction bipolar transistors*

The InGaP/GaAs/InGaP double heterojunction bipolar transistor structure is grown by chemical beam epitaxy (CBE) with all gaseous sources including doping sources [15] at 550°C: trimethylindium (TMIn), triethylgallium (TEGa), arsine (AsH_3), and phosphine (PH_3). Hydrogen is used as the carrier gas for the organometallic sources. The *p*-type carbon doping source is TMGa with hydrogen and the *n*-type doping source is H_2S. As shown in Fig. 2, the layer structure is grown

on semi-insulating GaAs substrate in the following sequence: 2500 Å undoped GaAs buffer layer, 2500 Å n^+-GaAs subcollector (2×10^{18} cm^{-3}), 4000 Å n^--InGaP collector (10^{17} cm^{-3}), 200 Å undoped GaAs setback layer, 850 Å p^+-GaAs base ($1{\cdot}2 \times 10^{19}$ cm^{-3}), 25 Å undoped GaAs setback layer, 2500 Å N^--InGaP emitter (10^{17} cm^{-3}), 2500 Å n^+-GaAs contact layer (2×10^{18} cm^{-3}), and 50 Å n^+-$In_{0.8}Ga_{0.2}As$ emitter contact layer (2×10^{18} cm^{-3}). Because of the small out-diffusion of carbon atoms from the base, a very small undoped base-setback layer of 25 Å is used. Transistors are fabricated with conventional photolithographic processes and wet chemical etching. Nonalloyed base contacts are used to reduce the excess recombination in the extrinsic base region.

		Å	cm^{-3}
n^+	$In_{0.8}Ga_{0.2}As$	50	2×10^{18}
n^+	GaAs	2500	2×10^{18}
N^-	$In_{0.49}Ga_{0.51}P$	2500	1×10^{17}
i	GaAs	25	—
p^+	C-GaAs	850	$1{\cdot}2 \times 10^{19}$
i	GaAs	200	—
N^-	$In_{0.49}Ga_{0.51}P$	4000	1×10^{17}
n^+	GaAs	2500	2×10^{18}
i	GaAs buffer SI GaAs	2500 substrate	—

640/2

Fig. 2 *Layer structure of InGaP/GaAs/InGaP double heterojunction bipolar transistors with carbon-doped base*

Undoped base setback layer is only 25 Å

The room-temperature common-emitter current–voltage characteristics of a carbon-doped InGaP/GaAs/InGaP DHBT with $10 \times 40\,\mu m^2$ emitter area is shown in Fig. 3. It shows a DC current gain of 120 with a very small collector saturation voltage (V_{CEsat}) of 75 mV. The collector breakdown voltage is 7 V which comes from the relatively thin and highly-doped collector region. The breakdown voltage can be further increased with a thicker and lightly-doped collector. The Gummel plot of the collector current and base current is shown in Fig. 4. A collector current ideality factor of 1·1 indicates a dominant thermionic electron injection process over the small InGaP/GaAs emitter–base heterojunction. The ideality factor of the base current is 1·6. The maximum current gain of 120 is obtained at a collector current density of 2 kA/cm^2. Current gain up to 18 is obtained at a low collector current of 10 μA which indicates excellent InGaP/GaAs emitter–base heterointerface and the effectiveness of nonalloyed base contact.

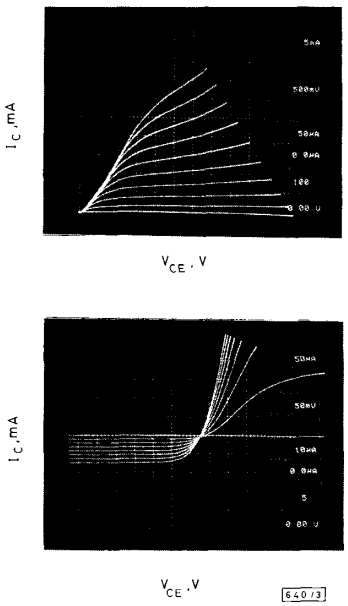

Fig. 3 *Room-temperature common emitter characteristics of InGaP/GaAs/InGaP DHBT with 14 × 40 μm² emitter area*

Collector saturation voltage is 75 mV

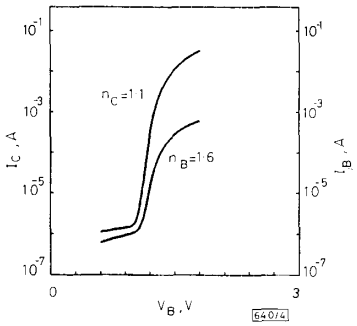

Fig. 4 *Room-temperature Gummel plot of carbon-doped InGaP/GaAs/InGaP DHBT*

Ideality factors are 1·1 and 1·6 for collector current and base current, respectively

In summary, we have fabricated InGaP/GaAs/InGaP double heterojunction bipolar transistors which exploit the large ΔE_V of the InGaP/GaAs emitter, the small ΔE_C of the InGaP/GaAs collector, and heavily-doped GaAs base with carbon using the CBE growth technique. With a 25 Å base setback layer, a current gain of 120 is obtained at J_C = 2 kA/cm^2. Nonalloyed base contact is demonstrated to preserve a current gain of 20 at $I_C = 10\,\mu A$.

6th April 1992

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References

1 ASBECK, P . M., CHANG, M. F., HIGGINS, J. A., SHENG, N. H., SULLIVAN, G. J., and WANG, K. C.: 'GaAlAs/GaAs heterojunction bipolar transistors: issues and prospects for application', *IEEE Trans.*, 1989, **ED-36,** pp. 2032–2042

2 KROEMER, H.: 'Heterostructure bipolar transistors and integrated circuits', *Proc. IEEE.*, 1982, **70,** p. 13

3 KROEMER, H.: 'Heterostructure bipolar transistors: what should we build?', *J. Vac. Sci. Technol. B*, 1983, **1,** pp. 126–130

4 MONDRY, M. J., and KROEMER, H.: 'Heterojunction bipolar transistor using a (Ga, In)P emitter on a GaAs base, grown by molecular beam epitaxy', *IEEE Electron Device Lett.*, 1985, **EDL-6,** pp. 175–177

5 KOBAYASHI, T. TAIRA, K., NAKAMURA, F., and KAWAI, H.: 'Band lineup for a GaInP/GaAs heterojunction measured by a high gain Npn heterojunction bipolar transistor grown by metalorganic chemical vapor deposition', *J. Appl. Phys.*, 1989, **65,** pp. 4898–4902

6 ALEXANDRE, F., BENCHIMOL, J., DANGLA, J., DUBON-CHEVALLIER, C., and AMARGER, V.: 'Heavily doped base GaInP/GaAs heterojunction bipolar transistor grown by chemical beam epitaxy', *Electron. Lett.*, 1990, **26,** pp. 1753–1754

7 DELAGE, S., DI FORTE-POISSON, M., BLANCK, H., BRYLINSKI, C., CHARTIER, E., and COLLOT, P.: 'First microwave characterisation of LP-MOCVD grown GaInP/GaAs aligned HBT', *Electron. Lett.*, 1991, **27,** pp. 253–254

8 WATANABE, M. O., and OHBA, Y.: 'Interface properties for GaAs/InGaAlP heterojunctions by the capacitance–voltage profiling technique', *Appl. Phys. Lett.*, 1987, **50,** pp. 906–980

9 BISWAS, D., DEBBAS, N., BHATTACHARYA, P., RAZEGHI, M., DEFOUR, M., and OMNES, F.: *Appl. Phys. Lett.*, 1990, **56,** pp. 833–835

10 CHEN, J. SITES, J. R., SPAIN, I. L., HAFICH, M. J., and ROBINSON, G. Y.: 'Band offset of GaAs/$In_{0.48}Ga_{0.52}P$ measured under hydrostatic pressure', *Appl. Phys. Lett.*, 1991, **58**, pp. 744–746
11 HAASE, M. A., HAFICH, M. J., and ROBINSON, G. Y.: 'Internal photoemission and energy-band offsets in GaAs-GaInP p-I-N heterojunction photodiodes', *Appl. Phys. Lett.*, 1991, **58**, pp. 616–618
12 KONAGAI, M. YAMADA, T., AKATSUKA, T., SAITO, K., and TOKUMITSU, E.: 'Metallic p-type GaAs and AlGaAs grown by MOMBE', *J. Cryst. Growth*, 1989, **98**, p. 167
13 ENQUIST, P., WICKS, G., EASTMAN, L. F., and HITZMAN, C.: 'Anomalous redistribution of Be in GaAs grown by MBE', *J. Appl. Phys.*, 1985, **58**, p. 4130
14 REN, F., FULLOWAN, T., LOTHIAN, J., WISK, P., ABERNATHY, C., KOPF, R., EMERSON, A., DOWNEY, S., and PEARTON, S.: 'Stability of carbon and beryllium-doped base GaAs/AlGaAs heterojunction bipolar transistors', *Appl. Phys. Lett.*, 1991, **59**, pp. 3613–3615
15 TSANG, W.: 'A review of CBE, MOMBE, and GSMBE', *J. Cryst. Growth*, 1991, **111**, pp. 529–538

HIGH-FREQUENCY PERFORMANCE FOR SUB-0·1 μm GATE InAs-INSERTED-CHANNEL InAlAs/InGaAs HEMT

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Indexing term: Microwave devices and components

The Letter examines the high-frequency performance of a sub-0·1 μm gate InAlAs/InGaAs HEMT with a thin InAs layer inserted into the InGaAs channel. The transconductance is 2·1 S/mm and the current-gain cutoff frequency is 264 GHz using a 0·08 μm-long gate.

InAlAs/InGaAs high electron mobility transistors (HEMTs) lattice-matched to InP substrates have demonstrated excellent high-frequency and low-noise performance, compared with AlGaAs/GaAs HEMTs [1–3]. The high performance is explained by the high electron mobility, saturation drift velocity, and sheet carrier density of the InAlAs/InGaAs two-dimensional electron gas (2-DEG) system.

Recently, we reported a 200 GHz cutoff frequency with a sub-0·25 μm gate length HEMT, and Mishra *et al.* reported a 250 GHz cutoff frequency with a 0·12 μm gate length HEMT. We also demonstrated that electron transport properties and device performances could be further improved using an InAlAs/InGaAs HEMT with a thin InAs layer inserted into the InGaAs channel (InAs-inserted-channel HEMT) [4].

In this Letter, we report the excellent high-frequency performance of the InAs-inserted-channel HEMT with a sub-0·1 μm gate length prepared using the T-gate fabrication process.

Fig. 1 shows the structure of the InAs-inserted-channel HEMT grown by molecular beam epitaxy (MBE) on a semi-insulating InP substrate. The InAs layer thickness L_w is 40 Å and the insertion position Z, the distance between the InAlAs spacer layer and the InAs layer, is 25 Å. The total thickness of the channel layer including the InAs layer is 300 Å. The doping density of the 50 Å InAlAs carrier-supply layer is $10^{19}\,cm^{-3}$. The planar-doped InAlAs layer, which was designed to reduce the source and drain series resistance, has a sheet doping density of $10^{13}\,cm^{-2}$.

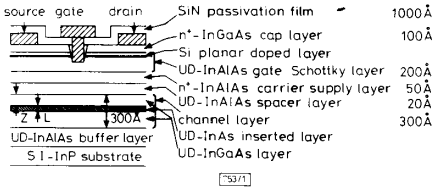

Fig. 1 *Device structure of InAs-inserted-channel HEMT*
UD: undoped

For the fabrication process, first, mesa etching for device isolation was carried out by ECR (electron cyclotron resonance) type RIE (reactive ion etching) using a mixture of Cl_2 and Ar gas. Ti/Pt/Au was deposited and lifted off to form the source and drain nonalloyed ohmic contacts. A T-shaped gate was formed using electron beam lithography as follows. After depositing an SiN passivation film 0·1 μm thick, the Schottky contact regions of the passivation layer were etched by RIE using a resist pattern formed by electron beam lithography as an etching mask. Next, the resist pattern for the gate-top portion was made by photolithography. Finally, after the gate recess etching, the gate metals of Ti/Pt/Au were deposited and lifted off.

The contact resistance R_c of the InAs-inserted-channel HEMT was determined to be 0·07 Ω mm by TLM measurement. The sheet resistance for the whole layer was 115 Ω/□. The source series resistance R_s of the InAs-inserted-channel HEMT was estimated to be 0·13 Ω mm.

Fig. 2 shows the current–voltage characteristics of the InAs-inserted-channel HEMT. Excellent pinchoff characteristics are obtained. The maximum extrinsic transconductance is ~2·1 S/mm at a drain bias of 2 V.

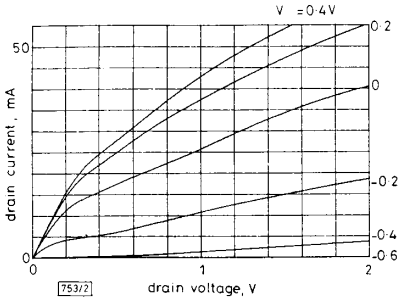

Fig. 2 *Current–voltage characteristics of 0·08 μm gate InAs-inserted channel HEMT with gate width of 50 μm*
Gate voltage ranges from −0·6 to 0·4 V

The current gain and the Mason unilateral power gain were derived from the S parameters. The S parameters were measured from 0·5 to 25·5 GHz. The current-gain cutoff frequency f_T and the maximum oscillation frequency f_{max} were calculated by extrapolating at −6 dB/octave. Fig. 3 shows the frequency dependence of the current gain and the Mason

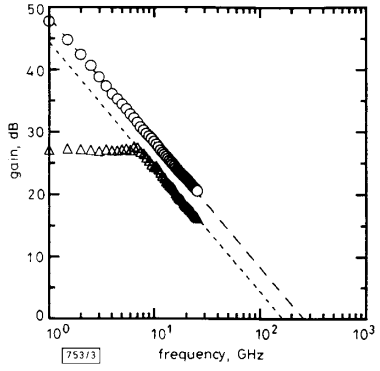

Fig. 3 *Current gain and Mason unilateral power gain against frequency for 0·08 μm-gate InAs-inserted-channel HEMT with gate width of 50 μm*
Gate bias is 0·05 V and drain bias is 0·75 V; f_T = 264 GHz, f_{max} = 166 GHz
○ current gain
△ Mason unilateral power gain